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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/009,768	01/20/1998	TAKAYUKI KIJIMA	PMS245024	7858

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EXAMINER

MOE, AUNG SOE

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 09/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/009,768

Applicant(s)  
Kijima et al

Examiner  
Aung S. Moe

Art Unit  
2612



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Jul 15, 2002.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above, claim(s) 1-13 and 25-37 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-24 and 38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on Jul 15, 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some\* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_ 6) ☐ Other:

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## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 14-24 and 38 have been considered but are moot in view of the new ground(s) of rejection.

With respect to Whipple '215, Applicant alleged that "Whipple '215 discloses execution of same color line addition by using a horizontal register provided for the addition operation." Thus, even combining Whipple '215 teachings with those of Parulski '406 does not result in the combinations defined by the present claimed invention such that "lines are added together in a vertical register" as amended.

In response, the Examiner respectfully disagrees because it is conventionally well-known that when the pluralities of lines from the solid-state image sensor are read out, they are normally added in the vertical register in order to attain a high-speed operation before transferred to the horizontal shift register and this is clearly evidenced by Whipple '215. In particular, Whipple '215 teaches that the pixel signals of n-line from the solid-state image sensor (i.e., see Figs. 3 & 5) are summed in the vertical register (36) before they are transferred to the horizontal shift register (38/40) (i.e., noted the BIN as shown in Fig. 5; col. 3, lines 15-20 of Whipple '215).

In view of the above, having the system of Parulski '406 which used the solid-state image sensor with the vertical shift registers (i.e., Fig. 2A of Parulski '406) and then given the well-established teaching of Whipple '215 wherein the charges read from the n-lines are summed in

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the vertical shift registers (i.e., see col. 3, lines 15-20), it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '406 as taught by Whipple '215, since Whipple '215 states at col. 1, lines 55+ that such a modification would provide a faster frame rate and increase sensitivity while decreasing image memory.

Therefore, the Examiner asserts that when considering the Parulski '406 and Whipple '215 references as a whole, the present claimed invention is obvious over the combination Parulski '406 and Whipple '215 for at least the reasons as discussed above.

Furthermore, the Applicant stated that "the imaging element according to Terada '888 is directed to a non-destructive read-out type imaging element (CMD) in an XY address, i.e., random access control system. Thus, this imaging element is based on the progressive read-out system, and is irrelevant in the drive principle to the non-destructive read-out type CCD."

In response, the Examiner respectfully disagrees because it is noted that the present claimed invention does require "the non-destructive read-out type CCD". In fact, the present claimed invention broadly states "a solid-state image sensor having a two-dimensional array of pixels" and such limitations are clearly disclosed by Terada '888 (see col. 8, lines 50-60 of Terada '888). Furthermore, Terada '888 teaches that the use of the CCDs image pickup device is also known in the art, the Applicant's attention is directed to col. 2, lines 24+ of Terada '888.

Furthermore, Parulski '597 clearly teaches the use of CCD image pickup device having a vertical shift registers and horizontal shift registers for reading the n-lines out of every 'm' lines within partially continuous k lines (i.e., Figs. 7A/7B and 10). Therefore, the combination of

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Terada '888 and Parulski '597 is clearly relevant to the solid-state image sensor used in an electronic imaging system (i.e., Camera) as broadly recited in the present claimed invention.

In view of the above discussion, the present claimed invention is further rejected as follows:

### *Claim Objections*

2. Claims 14-24 and 38 are objected to because of the following informalities:

In claim 14, it is unclear how "still picture recording" recited in claim 14, lines 11 relates to "still picture recording" recited in claim 14, line 8? If there is the same, the Examiner suggests changing "still picture recording" recited in line 11 in claim 14 to -- said still picture recording --.

In claim 15, it is unclear how "still picture recording or dynamic image processing" recited in claim 15, lines 11 and 13 relates to "still picture recording" recited in claim 15, line 8 or line 11? If there is the same, the Examiner suggests changing "still picture recording or dynamic image processing" recited in lines 13 in claim 15 to -- said still picture recording or said dynamic image processing-- and in line 11, please change "still picture recording or dynamic image processing" to -- said still picture recording or dynamic image processing --.

In claim 17, it is unclear how "each of n lines" recited in line 2 relates to "each of n lines" recited in claim 15, line 9+? If there is the same, the Examiner suggests changing "each of n lines" recited in lines 2 in claim 17 to --said each of n lines--.

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In claim 17, it is unclear how “still picture recording or dynamic image processing” recited in lines 3+ relates to “still picture recording or dynamic image processing” recited in claim 15, line 11? If there is the same, the Examiner suggests changing “still picture recording or dynamic image processing” recited in line 3 in claim 17 to -- said still picture recording or said dynamic image processing --.

In claim 20, it is unclear how “m lines” recited in line 5 of claim 20 relates to “m lines” recited in claim 15, line 10. If there is the same, the Examiner suggests changing “m lines” recited in line 5 in claim 20 to -- said m lines --.

In claim 38, line 10, please change “a plurality or vertical” to -- a plurality of vertical --.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 14, 16, 17, ~~18~~-19, 21-23 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al. (U.S. 5,828,406) in view of Whipple et al. (U.S. 5,926,215).

**Regarding claim 14**, Parulski '406 an electronic imaging system (Fig. 2) comprising:  
a solid-state image sensor (20) having a two-dimensional array of pixels capable of converting light incident thereon to electric signal (col. 3, lines 35+), the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another (i.e., see Fig. 3A); and

a color filter arranged on an incident plane of the solid-state image sensor (20) having a line sequential mosaic pattern (i.e., see Figs. 1A/1B and 4); and

control means (Fig. 1, the element 27) for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording (col. 6, lines 25+), and

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a mode for reading out pixel signal (i.e., noted the preview or motion mode) sums each of  $n$  lines ( $n \geq 2$ ,  $n$  being an integer) (i.e., noted from the Figs. 1 and 7, that the lines 1 and 2 are read out for the motion/preview mode and the read out signals are respectively combined at the output section of the solid-state image sensor 20; see col. 7, lines 15+, col. 8, lines 15+ and col. 9, lines 55-60) out of every  $m$  lines ( $m \geq 3$ ,  $m$  being an integer) (i.e., see Fig. 7, the lines 1-4 may be considered as the 'm' lines) within partially continuous  $k$  ( $k \geq 6$ ,  $k$  being an integer) lines of the solid-state image sensor (i.e., noted that the lines 1/2, 5/6, 11/12 and 15/16 are considered as the 'k' continuous lines) for still picture recording or dynamic image processing (i.e., the motion/preview mode).

Furthermore, it is noted that although Parulski '406 shows the solid-state image sensor (i.e., Fig. 3A) having a plurality of vertical registers (68) for transferring the pixel signals (66) to the horizontal shift register (70) during the operation of different operation modes (i.e., Still, & Motion/Preview), Parulski '406 does not explicitly state that the pixel signals are summed by utilizing a plurality of vertical registers as amended in present claimed invention.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Whipple '215. In particular, Whipple '215 teaches that the pixel signals of  $n$ -line of pixel signals read out from the solid-state image sensor (i.e., see Figs. 3 & 5) are summed in the vertical register (36) before they are transferred to the horizontal shift register (38/40) (i.e., noted the BIN as shown in Fig. 5; col. 3, lines 15-20 of Whipple '215).

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In view of the above, having the system of Parulski '406 which used the solid-state image sensor with the vertical shift registers (i.e., Fig. 2A of Parulski '406) and then given the well-established teaching of Whipple '215 wherein the charges read from the n-lines are summed in the vertical shift registers (i.e., see col. 3, lines 15-20), it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '406 as taught by Whipple '215, since Whipple '215 states at col. 1, lines 55+ that such a modification would provide a faster frame rate and increase sensitivity while decreasing image memory.

**Regarding claim 16**, Parulski '406 discloses in which the control means (i.e., Fig. 1, the element's 27) controls a mode of reading a plurality of k line blocks each of k lines in the whole lines (i.e., Figs. 5-7) for still picture recording or dynamic image processing (i.e., col. 6, lines 25+ and col. 7, lines 10+).

**Regarding claim 17**, Parulski '406 discloses in which image data obtained by reading out pixel signal sums each of n lines (i.e., noted the line 1 and 2 of the Fig. 7; see col. 9, lines 55-60) among m vertically continuous lines (i.e., noted the lines 1-4 of Fig. 7) for still picture recording or dynamic image processing, is such that its color signal is line sequential data (i.e., Fig. 4, col. 9, lines 5+ and lines 60+).

~~**Regarding claim 18**, Parulski '406 discloses in which the solid-state image sensor has a line sequential filter as color filter (i.e., Fig. 4).~~

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**Regarding claim 22**, Parulski '406 discloses in which dynamic image processed signal obtained in either of the above modes is used for AF, AE or AWB control data (col. 9, lines 1-10).

**Regarding claim 23**, Parulski '406 discloses in which dynamic image processed signal obtained in either of the above modes is used as AF, AE or AWB control data, and the AF, AE and AWB control data being calculated sequentially each in each frame (col. 4 lines 10+ and col. 9, lines 1+).

**Regarding claims 19 and 20**, it is noted that although Parulski '406 shows the use of color filters in which the n addition lines are constituted by the color filter (i.e., see Figs. 6a/6b and 7), and different n line addition filters are provided for every m lines (i.e., the R, G and B filter as shown in Figs. 4 and 7), Parulski '406 does not explicitly state that the n lines for addition are constituted by the same color filter as recited in claims 19 and 20.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Whipple '215. In particular, Whipple '215 teaches the use of the color filters in the electronic imaging system wherein the n lines for addition are constituted by the same color filter (i.e., Figs. 3 and 5).

In view of this, having a system of Parulski '406 and then given the well-established teaching of Whipple '215, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Parulski '406 as taught by Whipple '215, since Whipple '215 states at col. 2, lines 41+ that such a modification would provide a

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faster frame rate while preserve the color pixel pattern and effective field of view of the image sensor thereof.

**Regarding claim 21**, the combination of Parulski '406 and Whipple '215 shows in which  $m = 2^\infty + 1$  ( $\infty$  being a positive integer) (i.e., see Fig. 7 of Parulski '406 and Fig. 5 of Whipple '215).

**Regarding claim 38**, noted that claim 38 is rejected for the same reasons as set forth above for claim 14, please see the Examiner's comments with respect to claim 14 as discussed above.

5. Claims 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terada et al. (U.S. 6,124,888) in view of Parulski et al. (U.S. 5,668,597) and Udagawa et al. (U.S. 5,880,781).

**Regarding claim 15**, Terada '888 discloses an electronic imaging system (i.e., see Figs. 7-8 and 10) comprising:

a solid-state image sensor (i.e., Figs. 7/8, the element 103) having a two-dimensional array of pixels capable of converting light incident thereon to electric signal (i.e., see col. 2, lines 24+ and col. 8, lines 45+), the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another (i.e., see Fig. 8);

a color filter arranged on an incident plane of the solid-state image sensor having a line sequential mosaic pattern (Figs. 27A-28B; col. 26, lines 40+); and

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control means (Figs. 7 and 10; the elements' 109, 108 and 107) for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording (i.e., noted the "whole pixel mode" as shown in Fig. 15; see col. 11, lines 25+ and col. 13, lines 20+),

a mode (i.e., the "skip mode") for reading out pixel signals from some of the lines of the solid-state image sensor for still picture recording or dynamic image processing (i.e., noted the "block mode" as shown in Fig. 15 for motion image processing; see col. 11, lines 25+ and col. 14, lines 35+), and

a mode (i.e., the "block mode") for reading out pixel signals from some of the lines of the solid-state image sensor for still picture recording or dynamic image processing (i.e., noted the "block mode" as shown in Fig. 15 for motion image processing; see col. 11, lines 25+ and col. 13, lines 60+).

Furthermore, it is noted that the third to eight embodiments of Terada '888 does not explicitly state that the "skip mode" is performed by reading out pixel signals sums of  $m$  lines among  $m$  lines in  $k$  ( $k \geq 6$ ,  $k$  being an integer) continuous lines of the solid-state image sensor for still picture recording or dynamic image processing.

However, Terada '888 further teaches that the above mentioned claimed limitations are well-known in the art to modify the imaging system as disclosed in the third to eight embodiments. For example, Terada '888 teaches in the ninth embodiment (i.e., Figs. 25-27B) that in order to lower substantially the response of the opening and prevent the generation of the

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return strain (i.e., see col. 24, lines 35+ of Terada '888), it would have been obvious to modify the "skip mode" of the imaging system by reading out pixel signals sums of  $n$  lines among  $m$  lines in  $k$  ( $k \geq 6$ ,  $k$  being an integer) continuous lines of the solid-state image sensor for still picture recording or dynamic image processing (i.e., In Figs 27A, it is noted that lines 1 and 3 out of lines 1-3 are added to obtain the line 1 of Fig. 27, and wherein the total of more than 6 output lines may be provided for the motion image processing during the "skip mode"; see col. 26, lines 30+ and col. 28, lines 20+ of Terada '888).

Therefore, having the well-established teaching as discussed in the ninth embodiment of Terada '888, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the "skip mode" of the imaging system as shown in Fig. 7 as suggested in the ninth embodiment of Terada '888, since Terada '888 clearly states at col. 24, lines 36+ that such a modification would lower the response of opening and prevent the generation of the return strain thereof.

Furthermore, with respect to the "block mode", it is noted that although Terada '888 does not explicitly state the particular read out process, such that reading out pixel signal sums each of  $n$  ( $n \geq 2$ ,  $n$  being an integer) lines among  $m$  ( $m \geq 3$ ,  $m$  being an integer) lines of the solid-state image sensor, for still picture recording or dynamic image processing, such limitations are also well-known in the art as evidenced by Parulski '597.

In particular, Parulski '597 teaches (i.e., Figs. 1, 4 and 10) that the use of "block mode", wherein pixel signal sums each of  $n$  ( $n \geq 2$ ,  $n$  being an integer) lines among  $m$  ( $m \geq 3$ ,  $m$  being an

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integer) lines of the solid-state image sensor for dynamic image process (i.e., noted that the sum of each line 1 and 2 among the lines 1-4 of the pixel signals of block "66" may be read out as shown in Figs. 7A/7B and 10/11) so that the block of image signals may be read out for the purposed enabling rapid focus of the imaging system (i.e., see col. 3, lines 25+ and col. 7, lines 4+ of Parulski '597).

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Terada '888 as taught by Parulski '597, since Parulski '597 states at col. 3, lines 25+ that such a modification would decrease the required clock rate while enabling rapid focuses of the imaging system thereof.

Furthermore, it is noted that although the combination of Terada '888 and Parulski '597 discloses the solid-state image sensor having a plurality of vertical registers and horizontal shift register (i.e., see col. 2, lines 25+ of Terada '888 and Fig. 2A of Parulski '597) for reading out the pixel signals based on the different modes of operation (i.e., Noted the thin-out read-out modes, such as the block scanning, skip scanning, and whole pixel scanning as shown in Terada '888 and different operation mode such as preview modes, the Central area reading modes for focusing as shown in Figs. 4 and 5 of Parulski '597), the combination of Terada '888 and Parulski '597 does not explicitly state that the read-out pixel signal is summed by utilizing a plurality of vertical registers as amended in the present claimed invention.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Udagawa '781. In particular, Udagawa '781 teaches that in order to attain a high-

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speed thin-out reading operation and to obtain high image quality in an electronic imaging system, a color filter array is applied to a solid-state image sensor having a two-dimensional array of pixels (see col. 1, lines 40+) and reading out pixel signal sums of  $n$  lines (noted the elements' C1/M1 as shown in Fig. 2A) out of every  $m$  lines (i.e., noted the elements C1, M1, Y2, and G2) within partially continuous  $k$  lines (i.e., noted that the pixel signal of C1/M1 and C3/G3 lines are read out for every  $n$  lines of multi-pixel CCDs, thus, the value for ' $k$ ' is clearly greater than '6' as required by the claimed invention because CCDs having, e.g., 1.6 million pixels; see col. 1, lines 35+ and Fig. 6) of the solid-state image sensor (i.e., Fig. 6) by utilizing a plurality of vertical registers (i.e., the V-CCD; see Figs. 2A-2D and 6; col. 4, lines 30-45).

In view of this, having the combination of Terada '888 and Parulski '597 and then given the well-established teaching of Udagawa '781, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the imaging system of Terada '888 as taught by Udagawa '781, since Udagawa '781 clearly states at col. 2, lines 55+ that such a modification would provide a high-speed thin-out reading operation and high-image quality as obviously desired by the combination of Terada '888 and Parulski '597.

Regarding claim 24, the combination of Terada '888, Parulski '597 and Udagawa '781 discloses in which the control means (Fig. 7, the elements' 108, 106 and 107 of Terada '888) selects a mode of reading out pixel signal sums each of  $n$  lines among  $m$  vertical continuous lines when obtaining a dynamic image processed signal to be displayed on a display (i.e., the element

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106 of Terada '888) provided in it, to be supplied to an external display provided outside it or to be used as AE or AWB control data (i.e., see col. 1, lines 45+ of Udagawa '781), and

selects a mode (i.e., see Figs. 7, 10 and 15, the elements' 109, 108 and 107 of Terada '888) of reading out pixel signals of n lines among every m vertically continuous lines in k continuous lines (i.e., col. 28, lines 20+ of Terada '888) when obtaining a dynamic image processed signal to be used as AF or AE control data (i.e., col. 6, lines 25+ of Parulski '597 and col. 1, lines 45+ of Udagawa '781).

### *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nobuoka '569 shows an electronic imaging apparatus having a two-dimensional solid state sensor and operating with a different pixel read out operations thereof.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Any response to this final action should be mailed to:**

**Box AF**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**Or Faxed to:**

**(703) 872-9314**, (for formal communications; please mark "EXPEDITED PROCEDURE"; and for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,  
Arlington, VA., Sixth Floor (Receptionist).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Aung S. Moe** whose telephone number is **(703) 306-3021**. The examiner can normally be reached on Monday-Friday from 9:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wendy Garber**, can be reach on **(703) 305-4929**.

Any inquiry of a general nature or relating to the status of this application should be directed to the customer service number **(703) 306-0377**.

  
**AUNG S. MOE**  
**PATENT EXAMINER**

A. Moe

August 28, 2002